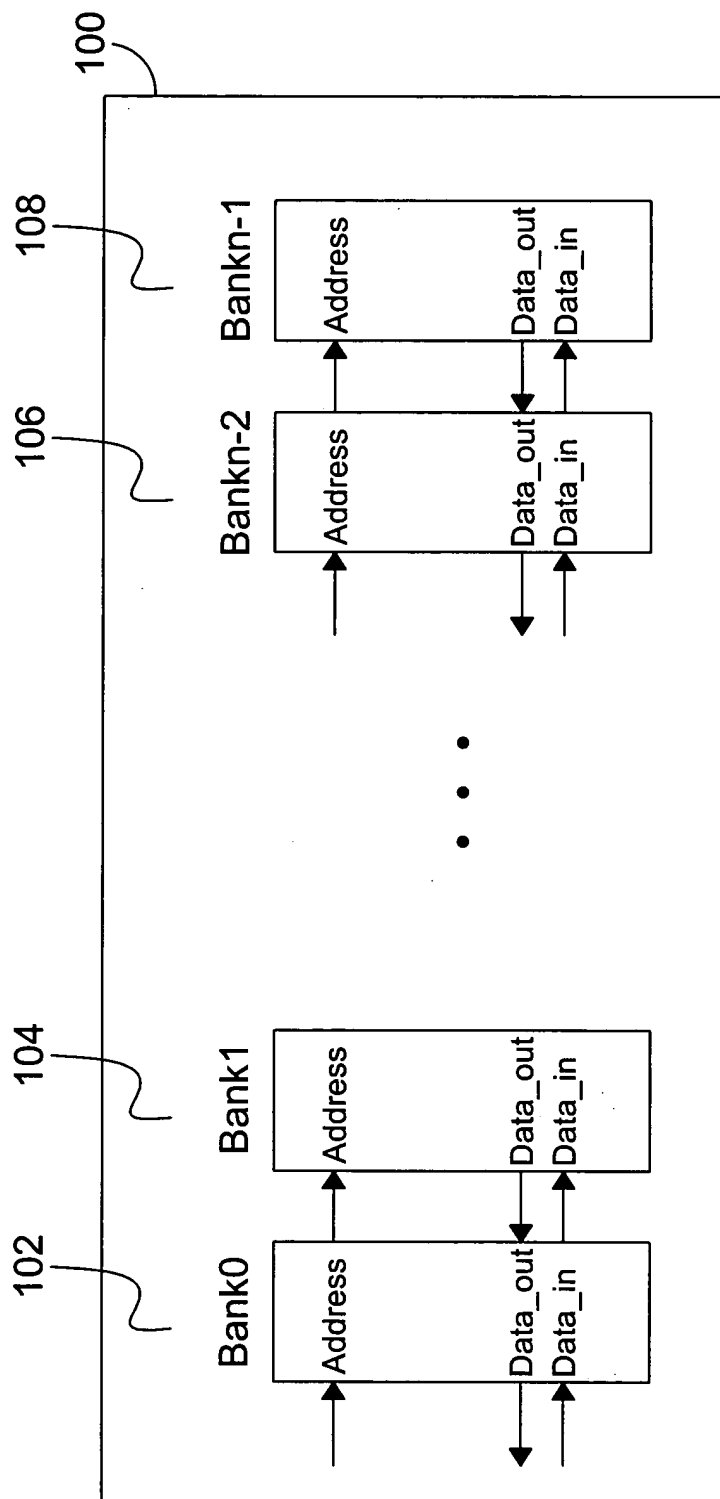




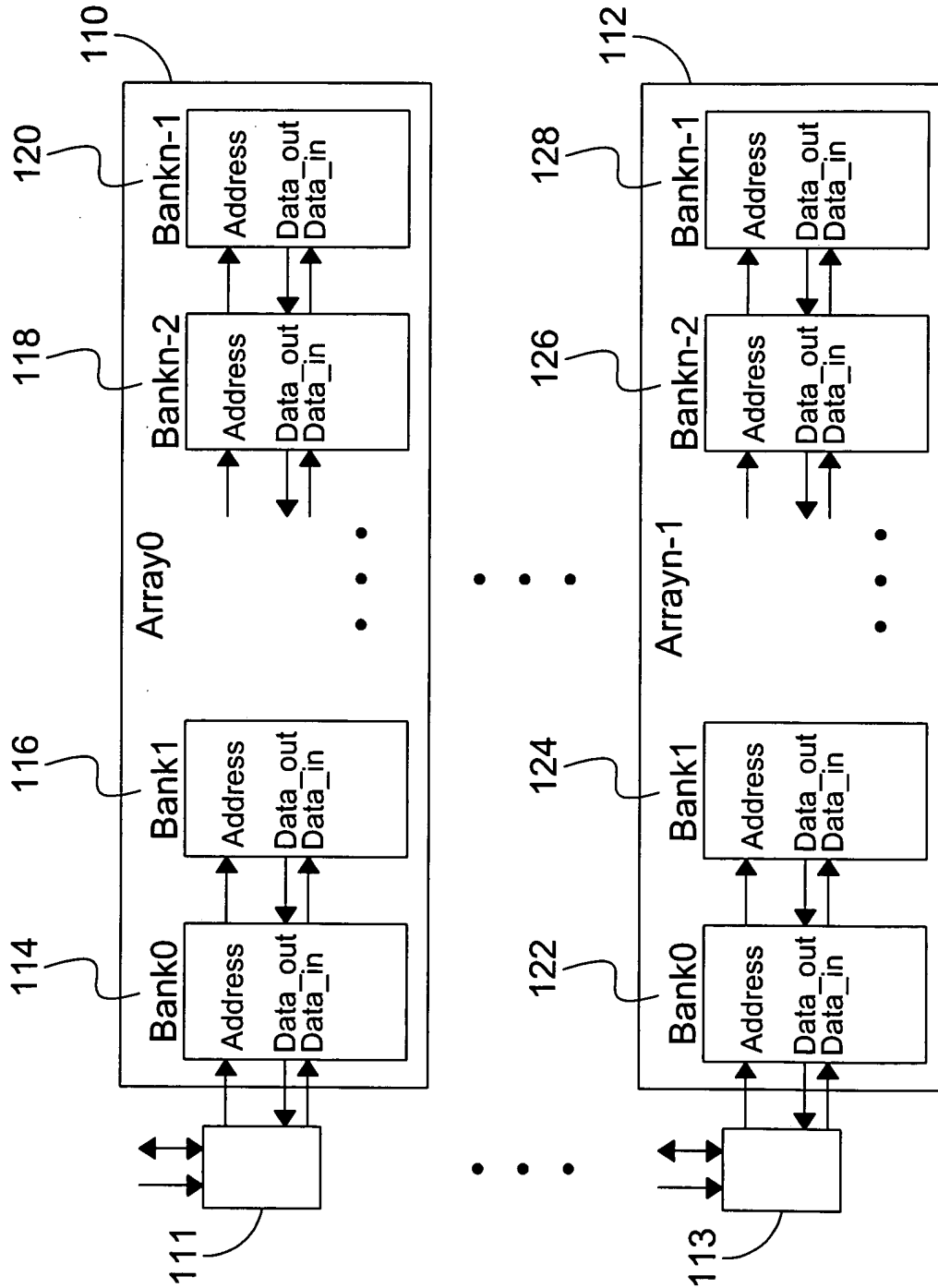
REPLACEMENT SHEET

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Pipelined Memory Array

FIG. 1(a)



Systolic Memory Array

FIG. 1(b)

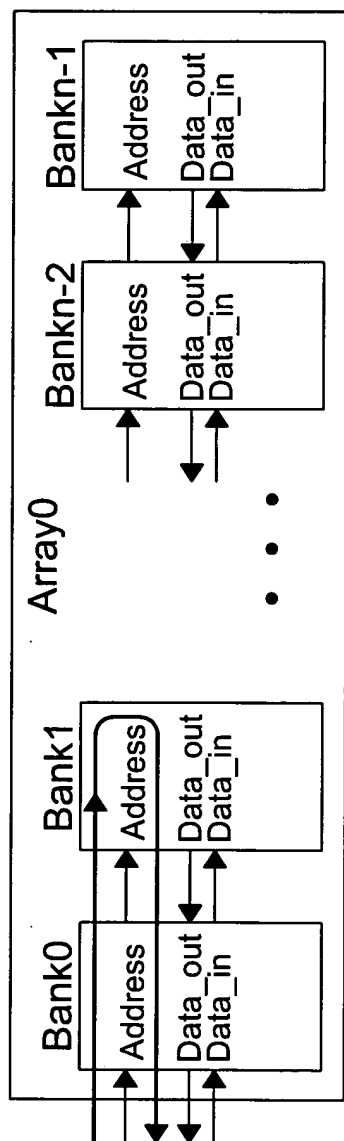


FIG. 2(a)

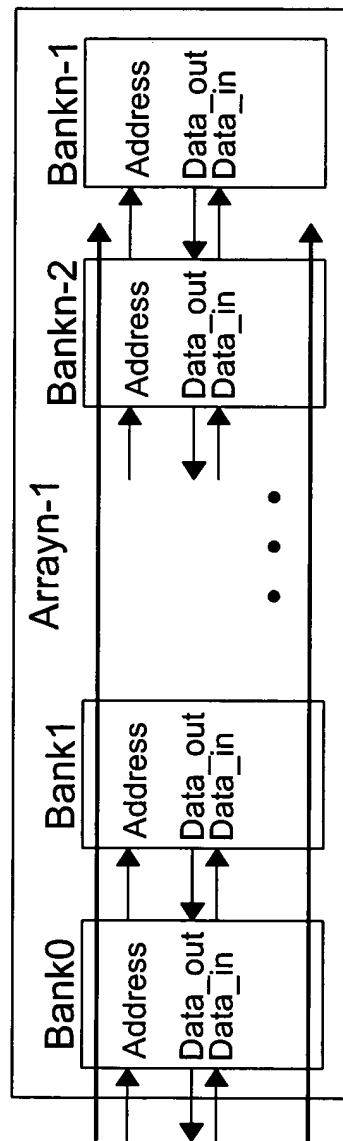


FIG. 2(b)

REPLACEMENT SHEET

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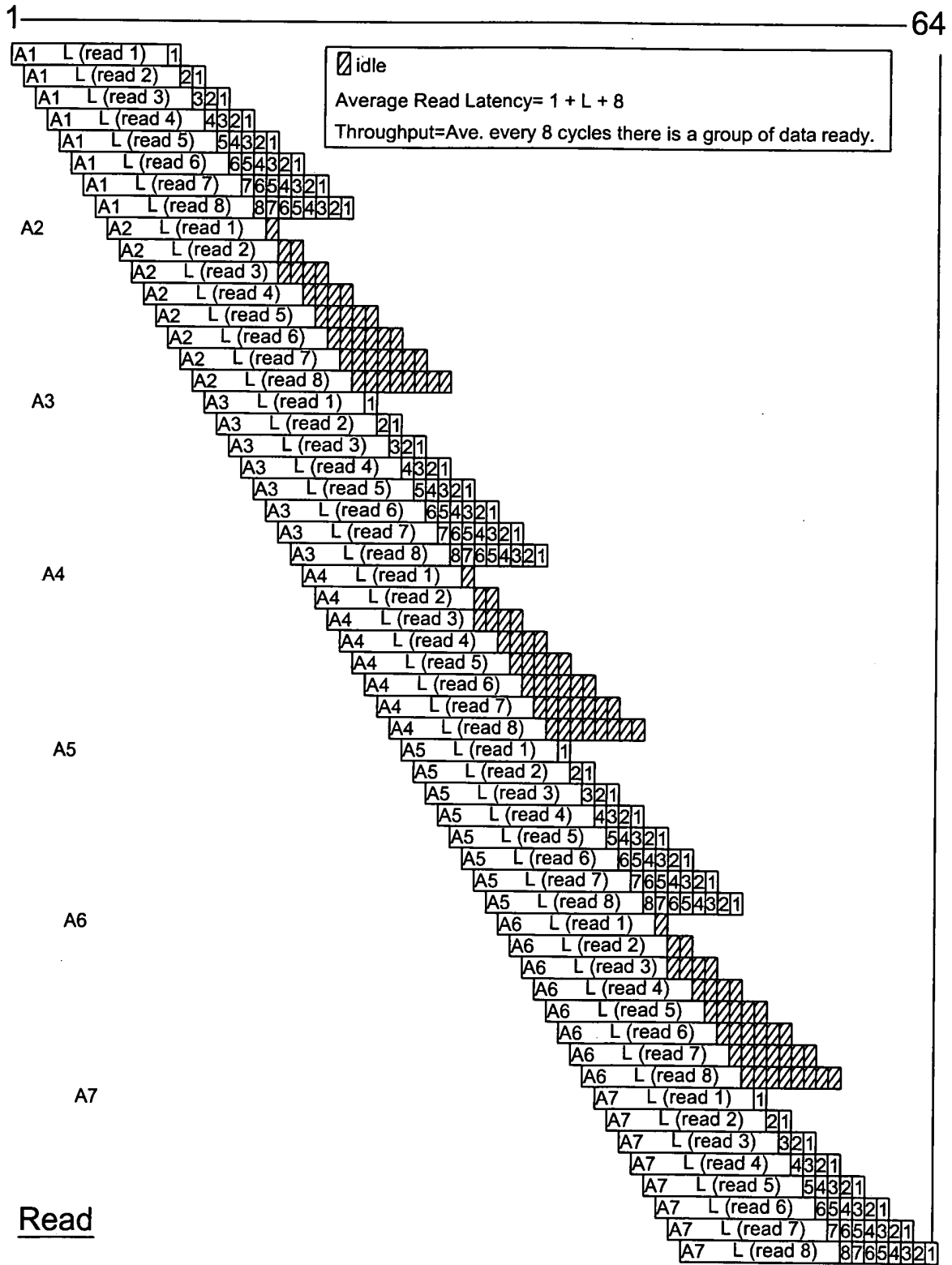


FIG. 3

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Write

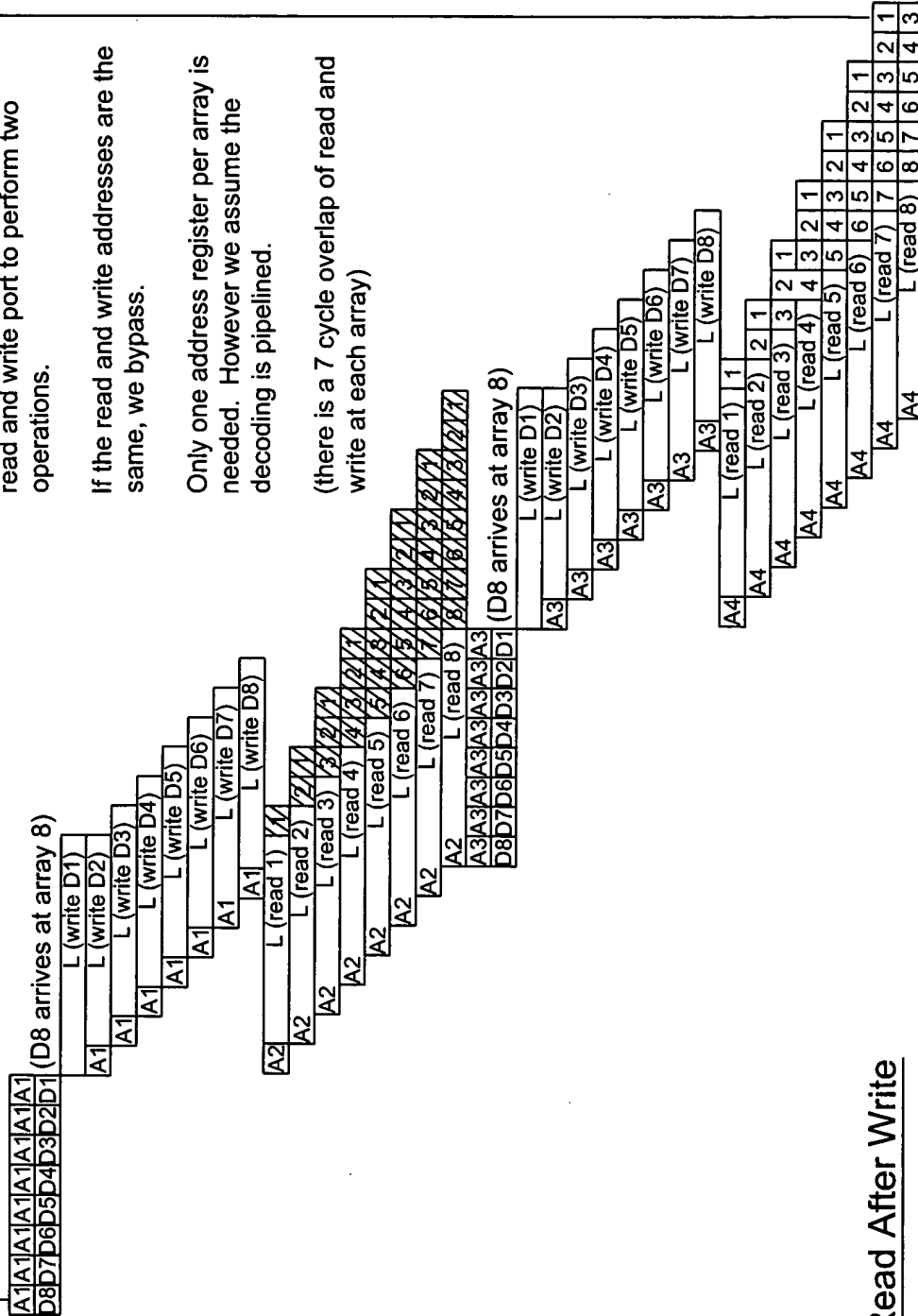
FIG. 4

We take advantage of the separated read and write port to perform two operations.

If the read and write addresses are the same, we bypass.

Only one address register per array is needed. However we assume the decoding is pipelined.

(there is a 7 cycle overlap of read and write at each array)

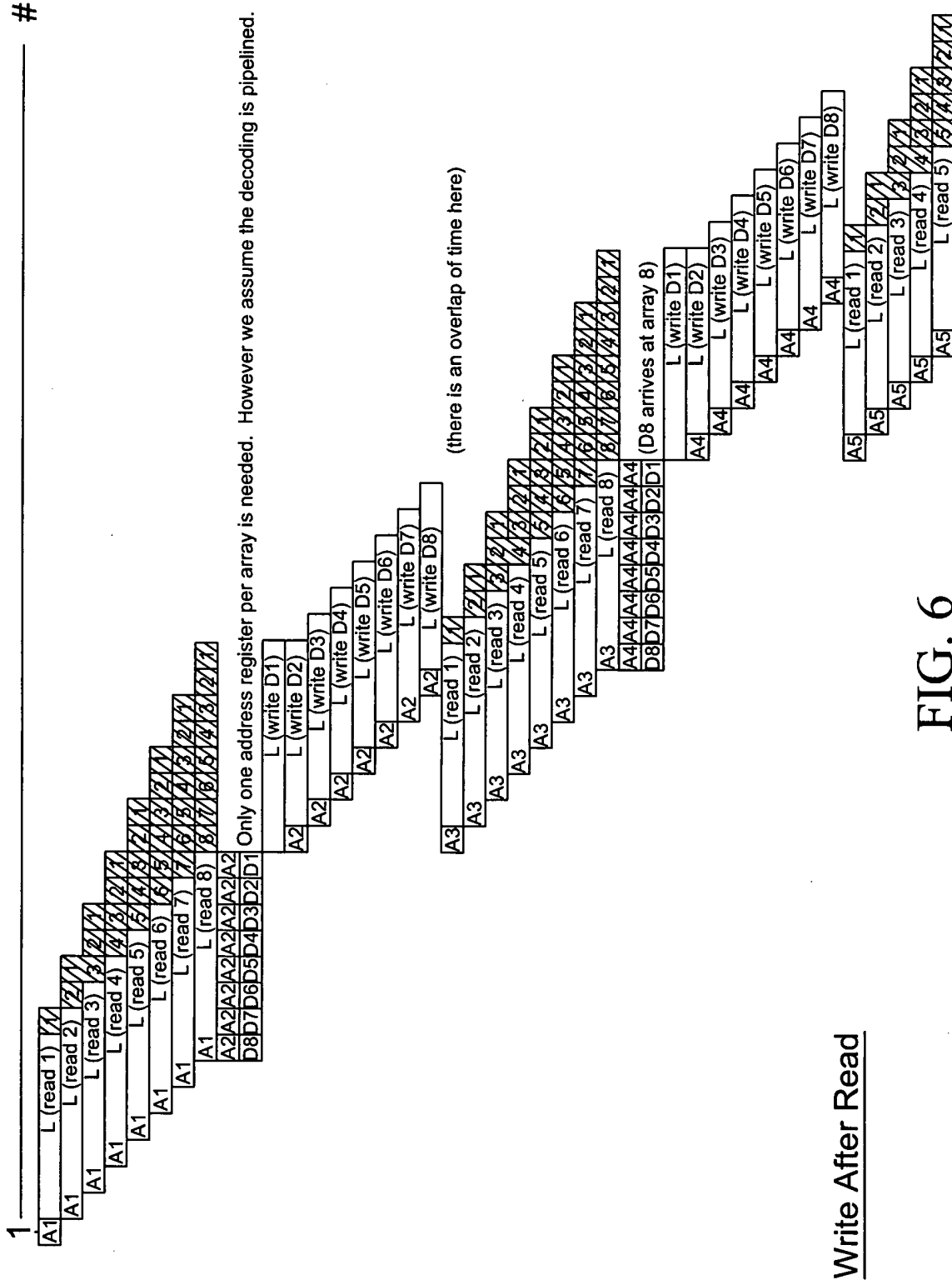


Read After Write

FIG. 5

REPLACEMENT SHEET

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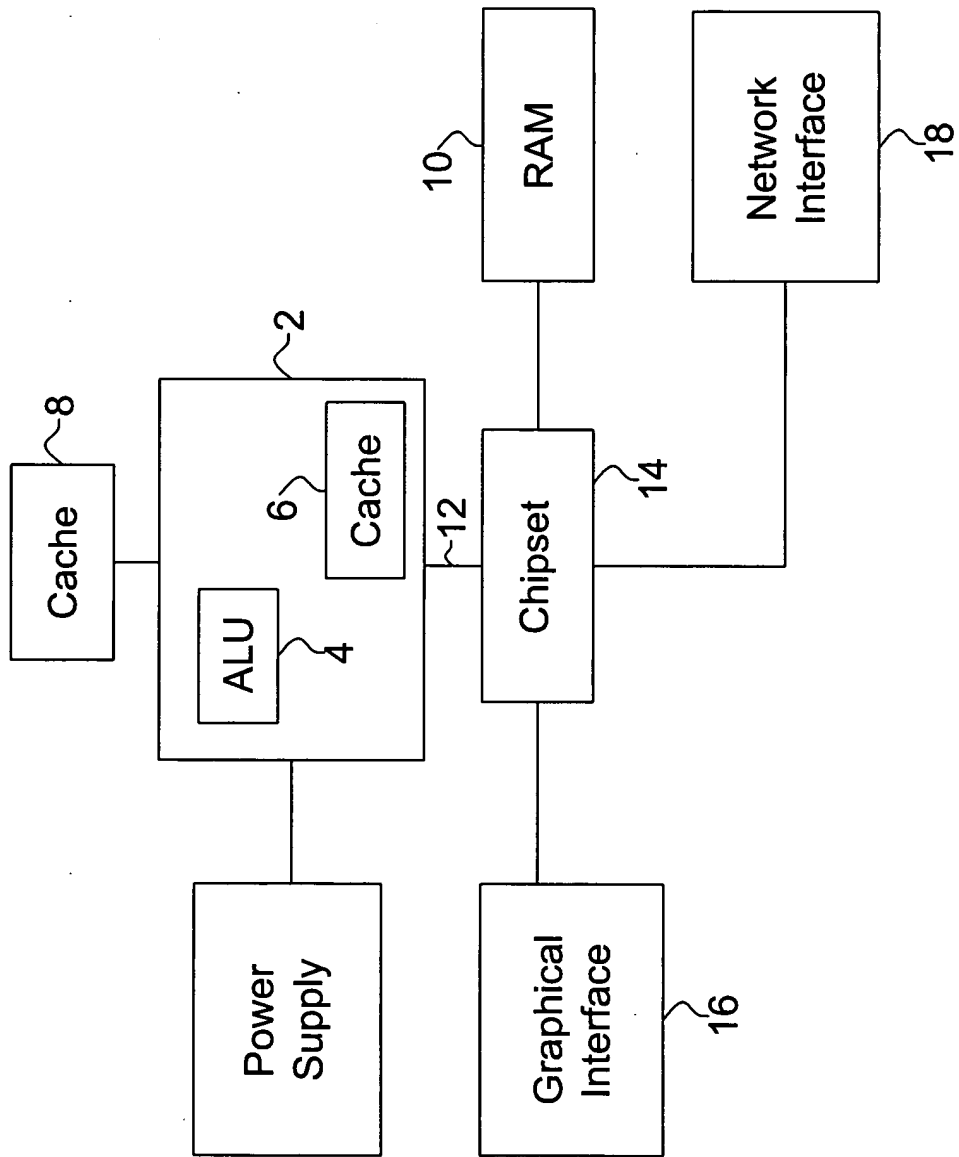


FIG. 7